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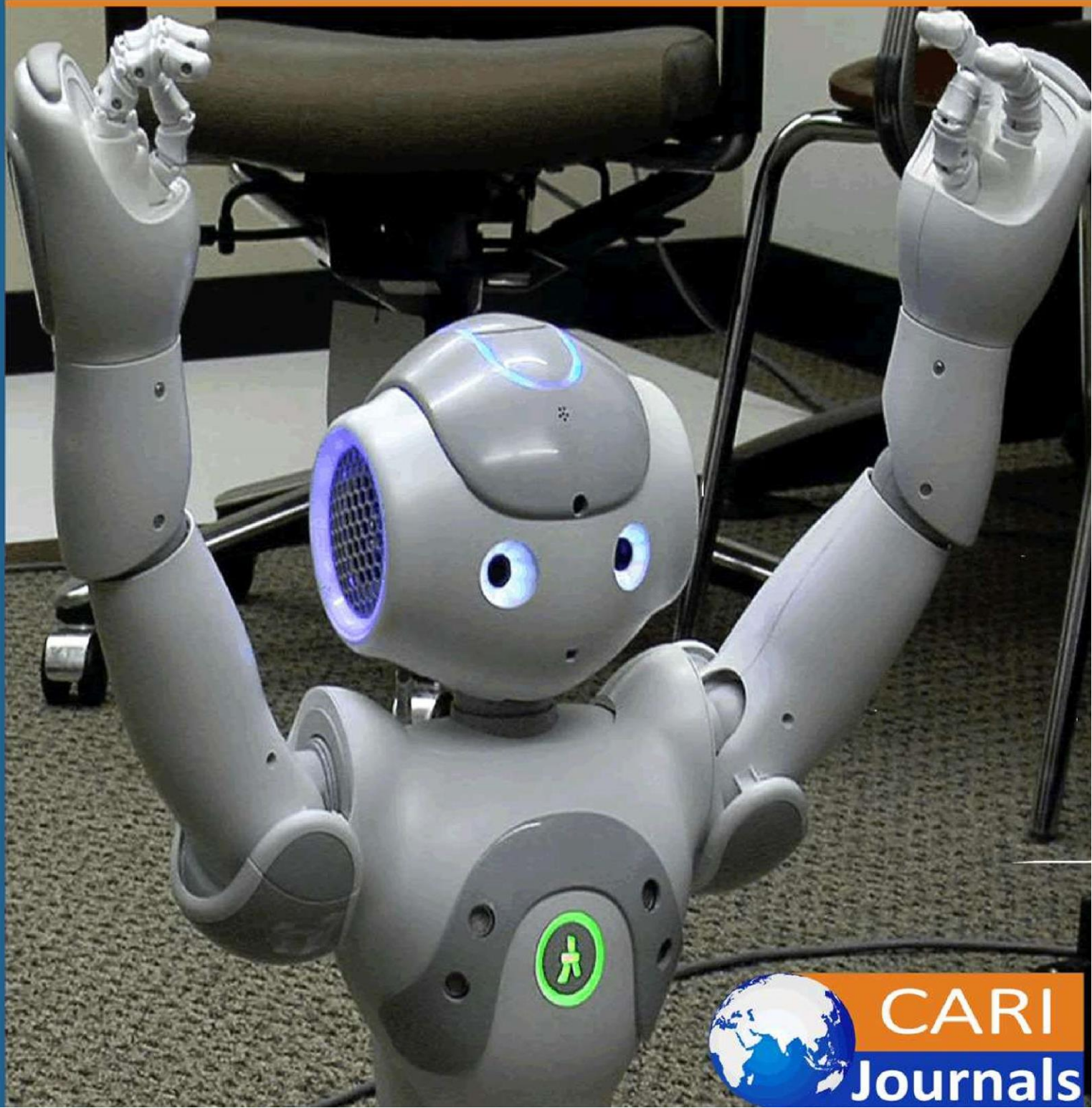

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Enhancing Semiconductor Functional Verification with Deep Learning with Innovation and Challenges

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Abstract

Purpose: Universally, the semiconductor is the foundation of electronic technology used in an extensive range of applications such as computers, televisions, smartphones, etc. It is utilized to create ICs (Integrated Circuits), one of the vital electronic device components. The Functional verification of semiconductors is significant to analyze the correctness of an IC for appropriate applications. Besides, Functional verification supports the manufacturers in various factors such as quality assurance, performance optimization, etc. Traditionally, semiconductor Functional verification is carried out manually with the support of expertise. However, it is prone to human error, inaccurate, expensive and time-consuming. To resolve the problem, DL (Deep Learning) based technologies have revolutionized the functional verification of semiconductor device. The utilization of various DL algorithms automates the semiconductor Functional verification to improve the semiconductor quality and performance. Therefore, the focus of this study is to explore the advancements in the functional verification process within the semiconductor industry.

Methodology: It begins by examining research techniques used to analyse existing studies on semiconductors. Additionally, it highlights the manual limitations of semiconductor functional verification and the need for DL-based solutions.

Findings: The study also identifies and discusses the challenges of integrating DL into semiconductor functional verification. Furthermore, it outlines future directions to improve the effectiveness of semiconductor functional verification and support research efforts in this area. The analysis reveals that there is a limited amount of research on deep learning-based functional verification, which necessitates further enhancement to improve the efficiency of functional verification.

Unique contribution to theory, policy and practice: The presented review is intended to support the research in enhancing the efficiency of the semiconductor functional verification. Furthermore, it is envisioned to assist the semiconductor manufacturers in the field of functional verification regarding efficient verifications, yield enhancement, improved accuracy, etc.

Keywords: *Semiconductor, Functional Verification, Deep Learning, Defect Detection, Convolutional Neural Network.*

1. INTRODUCTION

In the contemporary world, the semiconductor industry is composed of enormous innovations and growth that have made several developments in electronics [1]. The semiconductor is a significant electronic device component, enabling essential advancement in numerous sectors such as communications, health care, transportation, military, and countless other applications. Accordingly, it is significant to realize the impact of functional verification in semiconductor for verifying the design and improving the performance for suitable applications. Classically, it is functioned with the help of experts which takes time to process the verification outcome. Moreover, it is an expensive process, heavily dependent on resource skillset, expertise support and can be prone to manual error. To overcome the problem, DL-based technology revitalized semiconductor Functional verification, which enables the semiconductor industry in efficiency enhancement [2], design verification, and many more applications [3].

Correspondingly, several traditional methods planned to attain effective automation in the Functional verification of semiconductor. For instance, CNN based framework has been used for functional verification of semiconductor with fault detection and diagnosis mechanism. It has processed with the sensor data in the manufacturing of semiconductor. Besides, classical model detect faults directly from the variable length SVID (Status Variables Identification) data. The experimental outcome represents the better efficacy in the existing method [4]. Similarly, DL based mechanism has been used for the fault identification in semiconductor. Here, adaptation model has processed with the maximum mean discrepancy metric for enhancing the detection performance. Moreover, DCNN has been utilized for the feature extraction and with the real world semiconductor health condition monitoring dataset [5]. Likewise, enormous traditional models utilized various techniques in the functional verification of semiconductor.

Accordingly, projected study analyzes various DL-based frameworks in the semiconductor functional verification. Initially, it deliberates the necessity of the semiconductor functional verification. Besides, limitations of manual verification are signified to address the DL model requirement. Further, the evolution of the DL model in semiconductor Functional verification with verification techniques is represented in the study. Significantly, it depicts the challenges the researchers face in the semiconductor Functional verification and illustrates future directions to support the researchers in enhancing the semiconductor efficiency in appropriate requirements. The major contribution of the presented review is signified in the following:

- To represent advancements in the semiconductor Functional verification with DL techniques.
- To address the limitations faced by the existing research in the semiconductor Functional verification to support future research.
- To illustrate future directions in the semiconductor Functional verification to assist the researchers in enhancing semiconductor efficiency.

1.1. Paper Organization

The paper is organized as follows: section 2 discusses the review method, section 3 presents the overview of semiconductor functional verification, section 4 represents the evolution of DL in semiconductor functional verification. Correspondingly, section 5 illustrates the applications of DL in semiconductor functional verification.6 addresses the limitations faced by the existing research, section 7 defines the future directions and section 8 depicts the overall conclusion of the presented model.

2. RESEARCH TECHNIQUE

The systematic literature review is the fundamental scientific examination that collects abundant examination to produce an ample understanding the outcome of the research. The presented study started with the ideology of verification by accessing Google Scholar with specific keywords such as "semiconductor, functional verification," “deep learning," “defect detection," "convolutional neural network," etc. The presented study is composed of papers from the year 2020 to 2024 with recent advancements.

Search Strategy

The search plan of the study is introduced by the widespread selection of the databases. It is prearranged by selecting appropriate databases. Here, IEEE Access is the integrative electronic journal that delivers the advancements and outcomes of the original research. The following represents the sources utilized for the presented study.

1. Google Scholar [www.scholar.google.com.au/]
2. IEEE Access [https://ieeeaccess.ieee.org/]

Inclusion Criteria and Exclusion Criteria

This section depicts principles utilized to select papers for the analysis. Table 1 indicates the crucial parameter to collect the related papers.

Table. 1 Inclusion and Exclusion Criteria

S.No	Significant Parameters	Inclusion Criteria	Exclusion Criteria
1.	Years	Articles issued from 2020 to 2024	Articles issued before 2020
2.	Research Accomplished	Studies include of semiconductor Functional verification with DL technology	Studies associated with the process other than DL-based framework in semiconductor Functional verification
3.	Modality Kinds	Papers with DL-based approaches.	Paper without DL-based approaches.

3. SEMICONDUCTOR FUNCTIONAL VERIFICATION

The semiconductor Functional verification is the mechanism of investigating the quality and efficiency of the semiconductor or IC (Integrated Circuits) based on functionality. Generally, it includes analyzing electrical features, the ability of signal processing, errors in the design of semiconductors, patterns of semiconductors, etc. Accordingly, Functional verification assists in detecting the changes and problems that affect the function of the semiconductor devices. The Functional verification process based on the type of semiconductors. Consistently, the major objective of semiconductor Functional verification is to ensure that the devices meet particular requirements in order to improve semiconductor performance. It supports the semiconductor manufacturers in quality control, growth of product, troubleshooting, etc.

3.1 Limitations of Manual Semiconductor Functional Verification

The verification of functionality in semiconductor devices can be processed manually with the support of experts. Traditionally, it is processed with digital multimeter, oscilloscope, logic analyzers, utilization of power supplies and manually toggling switches. Conversely, it is prone to several drawbacks which affect the reliability of the semiconductor verification. The limitations of the manual verification are depicted in the following:

1. Manual error
2. Subjectivity
3. Time Invasive
4. Limited Scope of Automation
5. Inadequate Scalability
6. Expensive

Accordingly, manual verification is prone to human error which lacks accuracy in verification. Besides, diverse experts will lead to different interpretations of the verification which affects the quality of the verification. Similarly, it is a time-invasive process where the outcome of the verification takes time to progress by the experts. Moreover, handling larger sizes and complexity is challenging for manual verification. Besides, manual verification with the experts is an expensive process based on resources, time, and expertise. Furthermore, to resolve the problem, technologies are needed that automate the semiconductor examination.

4. EVOLUTION OF DEEP LEARNING IN THE SEMICONDUCTOR FUNCTIONAL VERIFICATION

The DL-based technique is a significant factor designed to automate the verification process in various electronic devices. In the Functional verification of semiconductors, traditional methods used diverse algorithms to investigate the efficiency of the semiconductor. Accordingly, DL techniques were primarily used in image recognition methods in semiconductor verification such as error identification and classification. It automates the verification, improving the accuracy and handling of complex patterns in semiconductor design [6]. Besides, it optimizes the semiconductors' manufacturing function, which supports the industry to increase the yield. It supports the manufacturers in the verification of semiconductor design and predictive maintenance.

Accordingly, the evolution of the DL technique in semiconductor Functional verification transformed the industry by allowing accurate verification and enhanced production quality. The following subsection depicts the mechanism used for the semiconductor Functional verification using DL algorithms.

4.1 Automatic Test Generation

The Automatic test generation in the semiconductor Functional verification utilizes the DL-based techniques to improve the test for examining the functions of the semiconductor.

In the conventional model, DL based fault detection and classification system has been designed in the traditional model. The major objective of the existing research has to identify abnormal events which cause defects in the semiconductor. Here, status variable identification data has used for the classification. The results of the classification represents better efficiency of the conventional approach [3]. Correspondingly, DL aided mechanism has been designed for the identification of threshold voltage of GAN HEMTS. Here, GA (Genetic Algorithm) has utilized for the prediction mechanism. It signifies the end to end process of automation in the optimization of semiconductor devices [7].

Congruently, automatic test generation for calculating the efficiency of the semiconductor is processed through the verification of the defects in the semiconductor. The semiconductor defects are inversely proportional to the efficiency and reliability of the semiconductor. The performance of the classification is generally calculated using the essential metric accuracy which computes overall accurateness in the verification.

4.2 Coverage Optimization

The coverage optimization in the Functional verification of the semi-conductor with the DL technique signifies the mechanism of enhancing the efficiency in verifying and testing the semi-conductor. It analyzes the behavior of semiconductors in functional testing where it detects the critical location in the semiconductor which is significant to be analyzed for ensuring the working of semiconductors in various circumstances.

In the existing approach, NN (Neural Network) is utilized for enhancing prediction accuracy and minimize output variability in gradient methods for cross sectional data. Besides, it recommend a method to assess variability in optimized input in semiconductor processing, focusing on power delay of industrial DRAM circuits and electrical parameter measurements. Moreover, it has targeted to attain lower output variance when compared to the single MLP (Multi-Layer Perceptron). The experimental outcome represents better efficacy (R^2) by 5.6 to 15.6% and output variance reduction by 73.0 to 81.6% [8].

4.3 Property Checking and Real-Time Fault Detection

The section depicts the property checking and real-time fault detection in the semi-conductor functional verification. Accordingly, property checking includes analyzing particular behaviors in the properties in the design of semiconductors. It examines if the semiconductor design meets the particular constraints.

A DL based model has been designed for the prediction of performance and optimization in the TEFT (Tunnel Field Effect Transistors). To attain this, it utilized GeSi/Si heterojunction double gate TFET. Besides, NN (Neural Network) model has been used for the prediction of efficiency and forecast of the design structure [9]. Similarly, automated fault inspection of the semiconductor has designed in the conventional model. Here, SH-DNN (Hybrid Multistage System OF Stacked Deep Neural Network) has been used which permits the localization of the finest structures among the pixel size in the computer pipeline. Besides, classification has the DNN. Moreover, it is focused on the level of detail in the task relevant area of interest. The better performance of the fault detection has signified through the results with the F1-Score up to 99.5% [10].

Correspondingly, real-time fault detection and property checking are intended to enhance the efficiency and reliability of the semiconductor.

5. APPLICATIONS

The DL model in the semiconductor Functional verification made several advancements in various industries and sectors depicted in this section. The following represents the semiconductor design/manufacturing industries which uses DL-based technology for functional verification.

- Intel Labs
- Cadence Design Systems
- RISC-V Verification Working Group

Intel Labs

The Intel labs is the research division in the Intel Company which produces innovations in several technologies like computer processors. It utilizes a DL based framework for the investigation of performance in the semiconductors. The tool leverages the DL algorithm for performing the verification with NLP and other techniques. It understands the requirements and produces appropriate verification. Consistently, DL allows the company to identify the problem and enhancements to be made to improve semiconductor efficiency.

Cadence Design Systems

Correspondingly, Cadence Design Systems is a company that specializes in EDA (Electronic Design Automation), which uses DL technology for the investigation of semiconductor reliability. The DL-based model [11].

RISC-V Verification Working Group

The RISC verification working group is a combined effort among the RISC-V community, which is intended to corroborate the RISC-V in terms of semiconductor designs. It is an ISA (Instruction set of Architectures) that permits an efficient design of customizable processors [12].

6. CHALLENGES IN SEMICONDUCTOR FUNCTIONAL VERIFICATION

The section represents the restrictions and challenges in the semiconductor functional verification. The major limitations of classical models in the Functional verification of the semiconductor are represented in the figure.

Figure.2 Limitations

The figure.2 signifies the drawbacks of the semiconductor functional verification. It is identified that the major limitations of classical research are data availability, interpretability, generalization, computational properties, and expert support.

Data Accessibility

Several conventional models used diverse methods for the semiconductor Functional verification where the DL mechanisms need data for training. The usage of diverse datasets and a combination of the different datasets in a single model is lacking in the conventional models.

Illustration

The DL-based design deliberates black boxes which makes it difficult to understand the reason ahead of the predictions. The absence of interpretability can be a drawback in the Functional verification of semiconductors.

Simplification

The existing researchers trained on a particular set of datasets where the simplification of the unseen scenarios is limited through the DL models. It will influence the reliability and efficiency of the semiconductor functional verification.

Computational Properties

The classical methods are limited through the computational properties because DL techniques are computationally rigorous and need processing methods to enhance the performance.

Single Analysis

The pioneering research mainly concentrated on error detection, where the semiconductor functions with various sources are lacking in the classical models [13, 14].

It is significant to deliberate the limitations while leveraging DL in the semiconductor Functional verification which will support enhancing the efficiency of the semiconductor.

7. FUTURE DIRECTIONS

The future directions in semiconductor Functional verification involve developments in DL techniques and the incorporation of developing technologies. The probable developments in the semiconductor Functional verification are signified in the figure.3.

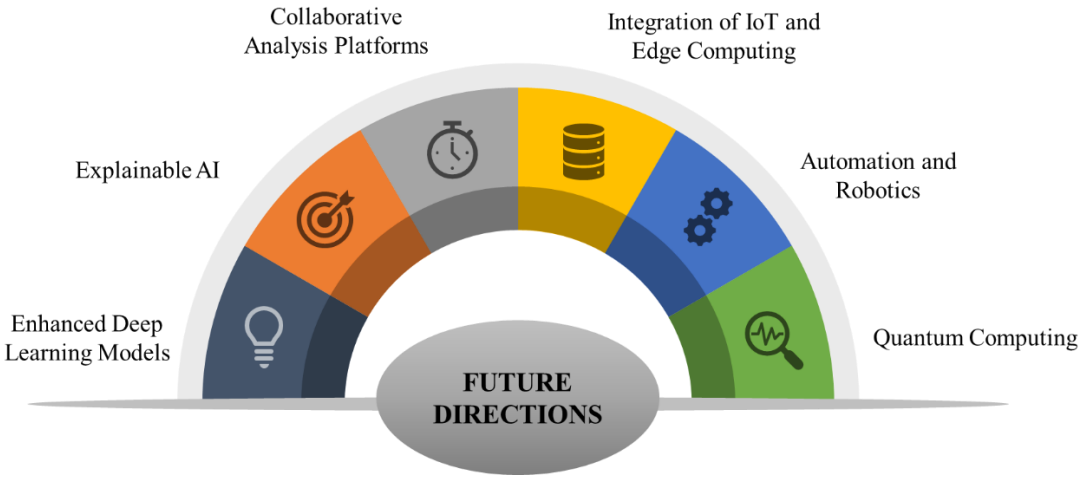

Figure.3 Future Research Imperatives

The figure.3 represents the future directions of the semiconductor functional verification. It is recognized that the probable enhancements are improved DL models, Amalgamation of edge computing and IoT-related technologies, quantum computing technology, a combination of verification platforms, robotics, and automation.

- The integration of enhanced DL models or a combination of DL mechanisms such as DCNN and LSTM will lead to improved design for the semiconductor functional verification. Besides, enhancing mechanisms such as data processing, feature extraction, etc, will boost the verification.
- The combination of advanced technologies with the DL will enhance the efficiency of the semiconductor Functional verification such as IoT and edge computing. It will ensure the real-time monitoring and functionality of the semiconductor verification.
- The utilization of enhanced technologies like quantum computing includes abilities to develop semiconductor functional verification. It assists the semiconductor manufacturing companies in resolving the challenging verification in the industry.
- The advancements in robotics will support the semiconductor Functional verification where the utilization of DL in the robotics technology transforms the verification in the semiconductor industry.

8. CONCLUSION

The development of semiconductors in the contemporary world supports several applications in various industries such as health care, military, etc. It is necessary to analyze the function of semiconductors to enhance their performance. The semiconductor Functional verification assists in the various factors in improving the efficiency of semiconductors such as design evaluation, defect detection, efficiency calculation, and much more. Traditional semiconductor Functional verification is processed with experts' help, which is time-consuming, expensive, and prone to human error. To tackle the problem, the DL bases model is used to automate the verification mechanism, which supports enhancing the accuracy of the semiconductor verification. The presented study addresses the recent advancements in DL-based semiconductor verification. Besides, it represents the challenges faced by conventional researchers in semiconductor functional verification. Furthermore, it depicts future directions to assist the researchers in developing models to enhance the semiconductor verification and performance.

… 9. RECOMMENDATIONS

Based on the analysis, it has been determined that only a limited number of studies have concentrated on semiconductor functional verification using DL technology. In today's era, it is crucial to prioritize DL technology in order to automate the manual processes involved in semiconductor functional verification. With many countries focusing on advancing the semiconductor industry, it is imperative to take the necessary steps to enhance functional verification through DL technology. Effective policy decisions should be made to serve as the determining factor in the progress of semiconductor functional verification with DL technology.

The following recommendations are provided for policymakers to enhance semiconductor functional verification:

- Increased Investment in semiconductor functional verification research and development
- Provision of skills Enhancement
- Establishment of a Regulatory framework
- Provision for incentives on innovation

These key factors are expected to significantly contribute to the improvement of DL-based semiconductor functional verification.

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